

# Design methodology of a non-invasive sensor to measure the current of the output capacitor for a very fast non-linear control

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**Abstract-** The combination of non-linear control and linear control proposed in [1] has a very fast transient response (voltage step from 1 V to 1.5 V in 2  $\mu$ s). In order to achieve this fast transient response the non-linear scheme is based on measuring the current of the output capacitor of a Buck converter. The design of this current sensor is complex due to parasitic effects such as component tolerances (bandwidth and dc gain of the Op-Amp), aging, temperature variation, etc. A design methodology for this current sensor is proposed regarding all these effects. The sensing circuit is designed to mirror the actual capacitor current with a trans-impedance amplifier by matching phase and scaling impedances of the RLC network (C, ESR and ESL of the output capacitor). The proposed methodology has been validated by means of a buck converter switching at 5 MHz. Experimental results validate that the current sensor behaves appropriately under voltage and load steps.

## I. INTRODUCCION

Nowadays the Voltage Regulator Modules (VRM) used in microprocessors and portable applications require high efficiency and fast transient response [2-3]. Fast dynamic control techniques can reduce the required output capacitor in this kind of applications, reducing the cost and the size of the solution. Different techniques have been presented in the literature to get fast transient response [1], [4-24]. The combination of non-linear and linear control presented in [1] achieves very fast transient response (voltage step from 1 V to 1.5 V in 2  $\mu$ s). Figure 1 shows the non linear and linear control scheme proposed in [1], it is based on a hysteretic control of the  $C_{out}$  current. When a load step occurs: the non linear control leads the converter close to the new steady state and the linear control provides the accurate regulation. In the literature many current sensors design can be found, most of them measure the current in the inductor or in the power MOSFET. (In [25], an overview of current sensing techniques is presented). The dynamic performance of this control technique is very good although to measure the output capacitor current is very complex. The use of a series resistance is not viable since the output impedance is deteriorated, worsening the dynamic response of the converter. The use of a current transformer is less invasive although output impedance is still affected. The

main disadvantages are the size, cost and integrating capability. Therefore, non-invasive technique must be used to avoid the increment of the  $C_{out}$  impedance, reduce size and keep integrating capability. The design of the non-invasive current sensor is difficult since it is very sensitive to parasitic effects.

This paper is organized as follows, section II explains the operating principle and design considerations, section III describes the proposed design methodology and design example. Section IV shows the experimental validation.

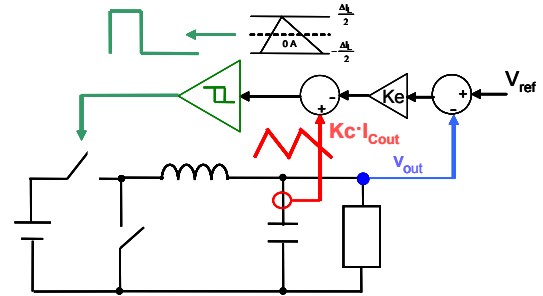


Figure 1. Linear and non-linear loop control scheme.

## II. OPERATING PRINCIPLE AND DESIGN CONSIDERATIONS

The RLC network is a non-invasive method to measure the current of the output capacitor ( $C_{out}$ ). The basic idea is to use an RLC network in parallel with the  $C_{out}$  (Figure 2) to measure the current by matching phases, time constants and impedance scaling. The current in the parallel network of the output capacitor is proportional to the  $C_{out}$  current (Figure 3).

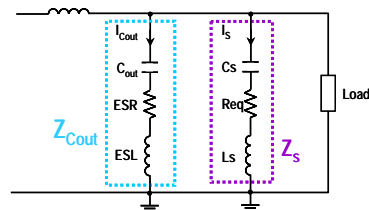


Figure 2. Capacitor current sensing method (RLC network).

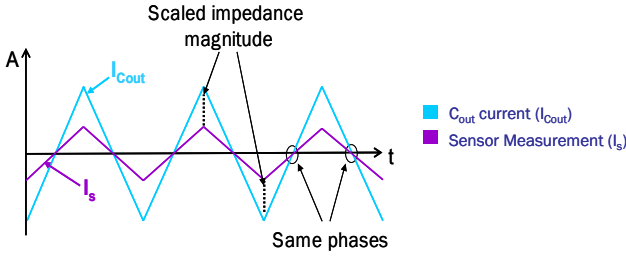


Figure 3. Matched phases and impedance scaling between sensor current ( $I_s$ ) and  $C_{out}$  current ( $I_{Cout}$ ).

#### A. Design limitation

The proper operation of this sensor strongly depends on the relative position of the converter switching frequency ( $f_{sw}$ ) and the  $C_{out}$  resonant frequency ( $f_{res}$ ). If  $f_{sw} > f_{res}$ , the  $C_{out}$  impedance presents inductive behavior (Figure 4). When  $f_{sw} < f_{res}$ , the impedance is capacitive. If the sensor is designed for the inductive side,  $f_{res}$  must be always lower than  $f_{sw}$  to guarantee the appropriate operation.

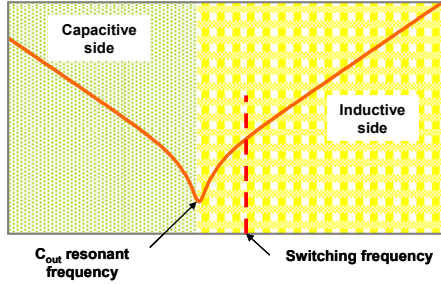


Figure 4. Impedance of the output capacitor.

If the  $C_{out}$  impedance behavior is different than expected (capacitive instead of inductive) due to the tolerance effects, the phase of the current changes drastically producing malfunctioning of the sensor. Figure 5 shows a sensor designed for inductive side, but if  $C$  is smaller (in this case 50% smaller) than expected the system changes from inductive to capacitive side. As a result of this  $C$  reduction: the real and measured currents are no longer in phase.

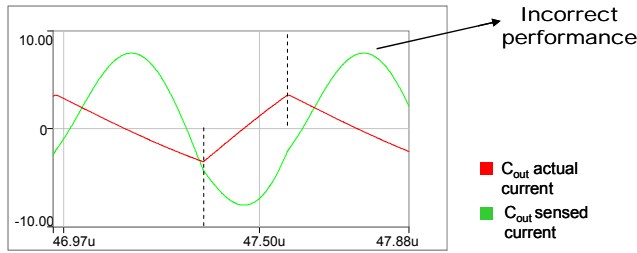


Figure 5. Measurement failure. Sensor designed for the inductive side, but  $C$  is smaller than expected.

The capacitance value is the output capacitor parameter most sensitive to tolerance effects like aging and dielectric material tolerances. The dielectric material affects the capacitance value in multilayer ceramic chip (MLCC) capacitor. For example, using X7R dielectric material tolerance is  $\pm 10\%$ , X5R changes

$\pm 20\%$  and Y5V changes  $+80\%$  and  $-20\%$  of the capacitance value.

Table 1 shows the influence of aging in ceramic capacitor. Temperature variation also affects the capacitance value ( $\pm 15\%$ ). These capacitance tolerances affect the resonant frequency. For example, for X7R dielectric material, Kyocera capacitor presents a  $-26\%$  reduction in capacitance value due to aging and temperature effects. This variation increases the resonant frequency 1.15 times higher (from 1.59 MHz to 1.8 MHz). And, Murata capacitor presents a  $-33\%$  reduction in capacitance value due to aging and temperature effects. This variation increases the resonant frequency 1.2 times higher (from 1.59 MHz to 1.9 MHz). Therefore, it is necessary to assure by design that system always operates in the same side.

Manufacturer	Dielectric	Variation after 10000 hours	
Murata	X7R	10%	Highest aging case
	Y5V, Z5U	15%	
	C0G	0%	
Kyocera	X7R	2%	Lowest aging case
	Y5V	15%	
Vishay	X7R	2.5%	
TDK	X7R	5%	
	Y5V	15%	
	C0G, X0H	0%	
AVX	X7R	6%	
RFE	X7R	5%	

Table 1. Ceramic capacitor aging from different manufacturers.

#### B. Design of parallel RLC network

The RLC network in parallel with output capacitor (to measure the current) is designed with the same time constants, equal phases and scaled impedance magnitude. The current through the parallel RLC network ( $I_s$ ) is proportional to the output capacitor current ( $I_{Cout}$ ) divided by the impedance scaling magnitude ( $n$ ). Equations (1), (2) and (3) should be accomplished in order to design an appropriate RLC network. Equation (1) shows the impedance scaling between the  $C_{out}$  and the parallel RLC network by  $n$  factor; equation (2) and (3) show the same time constants between the actual and mirror current.

$$n \cdot |Z_{Cout}| = |Z_s| \quad (1)$$

$$ESR \cdot C_{out} = R_{eq} \cdot C_s \quad (2)$$

$$ESL \cdot C_{out} = L_s \cdot C_s \quad (3)$$

#### C. Trans-Impedance amplifier

The actual implementation of the RLC network is based on a trans-impedance amplifier (Figure 6). The Op-Amp frequency behavior is assumed as a dc gain ( $A_{DC}$ ) with a pole at  $\omega_p$ , being  $\Delta B$  the Op-Amp bandwidth (Figure 6). The gain of the sensor ( $K_c$ ) is approximately given by equation (4).

$$K_c = -\frac{R1}{n} = \frac{\Delta V_s}{\Delta I_{Cout}} \quad (4)$$

The input impedance of the trans-impedance amplifier behaves as a resistive ( $R_i$ ) and inductive ( $L_s$ ) series network (Figure 7). This inductive (see equation 5) behavior is required to match the ESL effect of the output capacitor (Assuming that  $f_{sw} < \Delta B/10$ ). The input resistance ( $R_i$ ) behavior (see equation 6) of the trans-impedance amplifier is required to match  $R_s$  with the  $R_{eq}$  of the RLC network. The relationship between the  $R_{eq}$ ,  $R_i$  and  $R_s$  is given by equation (7).

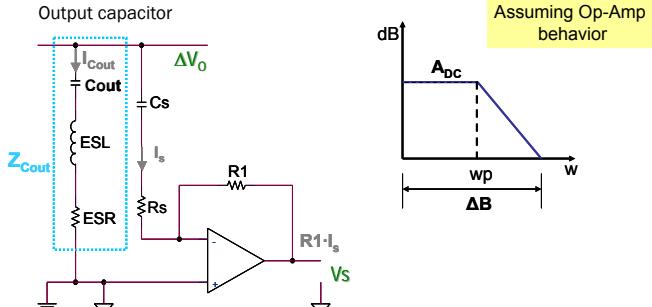


Figure 6. Physical implementation of the capacitor current sensing method (RLC network).

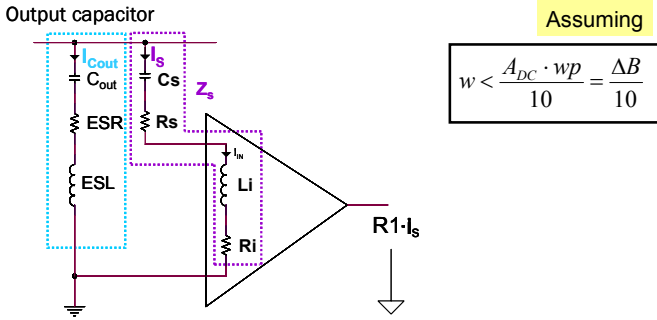


Figure 7. Equivalent circuit of the trans-impedance amplifier. The input impedance of the Op-Amp presents inductive behavior ( $L_i$ ).

$$L_s = \frac{R1}{\Delta B} \quad (5)$$

$$R_i = \frac{R1}{A_{DC}} \quad (6)$$

$$R_s = R_{eq} - R_i \quad (7)$$

#### D. Practical design considerations: Internal stability analysis

The design of this current sensor is sensitive to tolerances of bandwidth and dc gain of the Op-Amp. Figure 8 shows the range of  $\Delta B$  and  $A_{DC}$  variation for a specific Op-Amp (AD8061). For example, -15%  $\Delta B$  tolerance of the Op-Amp generate -15%  $f_{sw}$  variations. The temperature also modifies the bandwidth of the Op-Amp. For example, decrement of temperature (from 25 °C to -55 °C) results on approximately +6.4% of  $\Delta B$  increment. An increment of temperature (from 25 °C to 125 °C) results on approximately -1.6% of  $\Delta B$  decrement. Figure 9 shows for a specific Op-Amp (LM6171) how the temperature affects the value of the  $\Delta B$ .

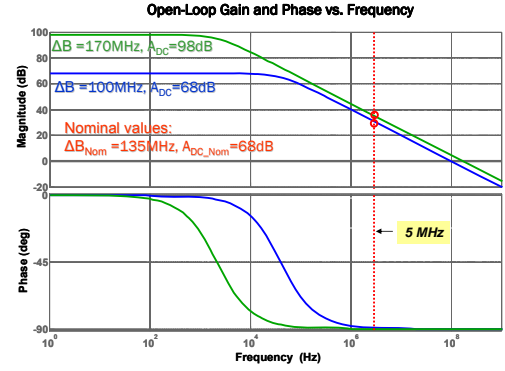
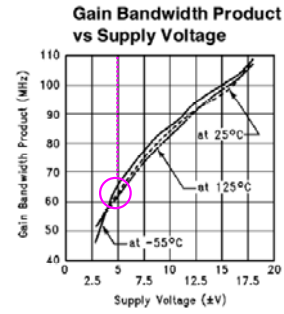


Figure 8. Frequency response of Op-Amp: AD8061. Maximum and minimum bandwidth and  $A_{DC}$  according to data sheet.



$\Delta B$  variation (Temperature) = +6.4%  $\Delta B$  (decrement from 25 °C to -55 °C) and -1.6%  $\Delta B$  (increment from 25 °C to 125 °C).

Figure 9. Tolerance of the Op-Amp bandwidth. LM6171.

The design methodology must also guarantee the internal stability of the Op-Amp (Figure 10), being:

$$\beta^{-1} = \frac{(R1+R_s) \cdot C_s \cdot s + 1}{R_s \cdot C_s \cdot s + 1} \quad (8)$$

$$f_z = \frac{1}{2 \cdot \pi \cdot (R1+R_s) \cdot C_s} \quad f_p = \frac{1}{2 \cdot \pi \cdot R_s \cdot C_s} \quad (9)$$

where,  $f_p$  is the pole and  $f_z$  is the zero of the  $1/\beta$  transfer function. The  $f_z$  and  $f_p$  do not depend of the “n” value.

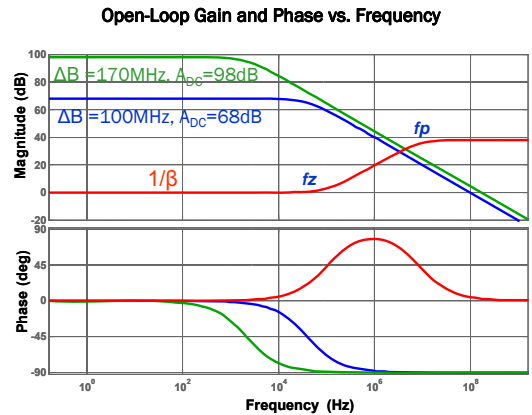


Figure 10. Op-Amp: Internal stability analysis.

### III. PROPOSED DESIGN METHODOLOGY AND DESIGN EXAMPLE

The design methodology for the current sensor is presented in this section, being applied in a design example. The objective of the design methodology is to obtain the value of  $K_c$ , to select the appropriate operational amplifier (Op-Amp), and to determine the  $R_s$  and  $C_s$  parameters. Also the impedance scaling magnitude ( $n$ ) will be obtained although it is and intermediate step.

The input specifications for the design example are:  $V_{in} = 3$  V,  $V_{out} = 1$  V,  $C_{out} = 4$   $\mu$ F (4.1  $\mu$ F),  $ESR = 4.5$  m $\Omega$ ,  $ESL = 450$  pF and  $f_{sw} = 5$  MHz. The proposed design methodology is based on the following steps:

**1.- Determine the range for the sensor gain ( $K_c$ ):** The value for the parameter  $K_c$  must be found within a range defined by  $K_{c_{Min}}$  and  $K_{c_{Max}}$ . These limits of  $K_c$  are chosen in order to assess that the gain of the trans-impedance amplifier is approximately the ideal gain ( $-R1$ ). This limit gives a minimum value for the sensor gain ( $K_{c_{Min}}$ ). And the maximum value of  $K_c$  ( $K_{c_{Max}}$ ) should be selected in order to ensure the small signal behavior of the Op-Amp (small signal bandwidth), this is, the output voltage ripple ( $\Delta V_s = K_c \cdot I_{C_{out}}$ ) must be low enough to assess the small signal frequency response of the Op-Amp. It is important to highlight that the value of the parameter  $K_c$  depends on the selected Op-Amp. The higher the Op-Amp bandwidth, the higher the sensor gain. The range of  $K_c$  for this example is  $0.14$  V/A  $< K_c < 2$  V/A.

**2.- Determine the appropriate Op-Amp:** The selection of the Op-Amp should accomplish the limits of the  $\Delta B$  and  $K_c$  in order to maintain the sensor working in the same side. The characteristics of the selected Op-Amp should accomplish: the minimum value of the bandwidth ( $\Delta B_{Min}$ ) that guarantee the internal stability and the ideal gain of the Op-Amp ( $V_s/I_s = -R1$ ). The maximum value of the bandwidth ( $\Delta B_{Max}$ ) should accomplish that the resonant frequency of the sensor ( $f_{res\_sensor}$ ) should be less than the switching frequency ( $f_{sw}$ ), keeping the sensor operation in the inductive side. The range of  $\Delta B$  for this example is  $102$  MHz  $< \Delta B < 237$  MHz. The bandwidth of the selected Op-Amp should be between the  $\Delta B_{Min}$  and  $\Delta B_{Max}$ . For a selected Op-Amp the  $K_c$  value is fixed and it does not depend on the  $n$  value. This  $K_c$  value should accomplish the range of  $K_c$ . For this design example the  $K_c$  value is equal to  $1/2.56$  V/A. The selected Op-Amp is AD8061, the  $\Delta B$  is equal to  $135$  MHz and the  $A_{DC}$  is equal to  $68$  dB.

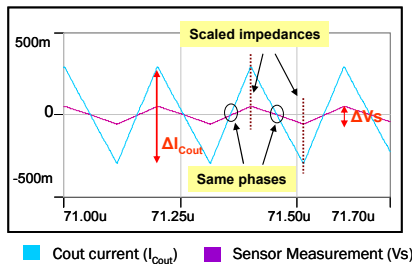


Figure 11. Simulation of designed sensor. Same phase, time constants and impedance scaling between  $V_s$  and  $I_{C_{out}}$ . Sensor designed for  $135$  MHz and  $A_{DC}$  of  $68$  dB.

**3.- Determine the range of the impedance scaling magnitude ( $n$ ):** The range of the impedance scaling magnitude ( $n_{Min} < n < n_{Max}$ ) should be selected in order to reduce the influence of parasitic on  $R_{eq}$  and  $C_s$  and in order to limit the parasitic effects of the Op-Amp (input capacitance and input bias current).

For the design example the range of the “ $n$ ” value is:  $1000 < n < 26500$ .

**Design considerations:** The  $R_{eq}$  value should be at less tens of ohms (in order to reduce the influence of  $R_i$ ) and  $C_s$  value should be at less hundreds of pF (in order to reduce the influence of parasitic effects).

**4.- Select the impedance scaling ( $n$ ):** The value of the parallel RLC network is given by equations (1), (2) and (3). For a given output capacitor ( $C_{out}$ ,  $ESL$  and  $ESR$ ) and switching frequency, the parallel RLC network depends only on parameter  $n$ . For each “ $n$ ”, there is only one value for  $R_{eq}$ ,  $C_s$  and  $L_s$ . The “ $n$ ” value should be selected in order to have a reasonable value of the parallel RLC network ( $C_s$ ,  $R_{eq}$  and  $L_s$ ).

The “ $n$ ” value for the design example is equal to  $10000$ . The parallel RLC network that accomplishes the design methodology is composed of  $C_s = 400$  pF,  $L_s = 4.4$   $\mu$ H,  $R_{eq} = 48$   $\Omega$ ,  $R1 = 3.7$  k $\Omega$ ,  $R_i = 1.5$   $\Omega$  and  $R_s = 47$   $\Omega$ .

*Simulation results and tolerance analysis (Influence of different  $\Delta B$  and  $A_{DC}$ )*

The design methodology is validated by simulation. The influence of the variation of  $\Delta B$  and  $A_{DC}$  in the performance of the sensor has been analyzed by simulation. These variations produce different time constants between the sensed current and  $C_{out}$  current. In spite of these variations a robust system is obtained. Figure 11 shows the validation of the current sensor design, this validation is done by simulation, it shows that both signals are in phase, scaled amplitudes and the peaks of the waveforms are in phase.

However, the design of this current sensor is sensitive to tolerances of bandwidth and dc gain of the Op-Amp. Figure 12 and Figure 13 show the current sensor designed for  $135$  MHz but, the real  $\Delta B$  of the Op-Amp is  $100$  MHz and  $170$  MHz respectively. These figures show that different bandwidth produces different constant times, but the peaks of the triangular waveform are in phase (Figure 12 and Figure 13). Finally variation in dc gain of the Op-Amp produces a negligible effect in  $K_c$  value (Figure 14).

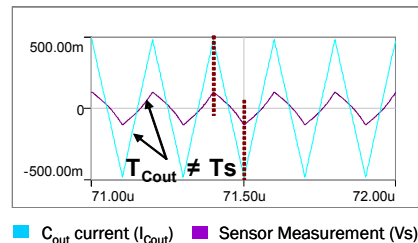


Figure 12. Sensor designed for  $135$  MHz but  $\Delta B$  of the Op-Amp is  $100$  MHz.



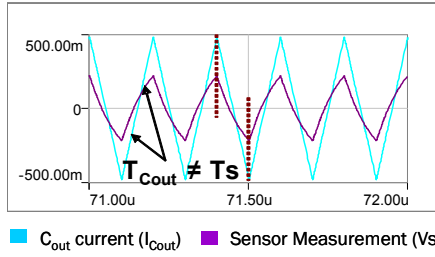


Figure 13. Sensor designed for 135 MHz but  $\Delta B$  of the Op-Amp is 170 MHz.

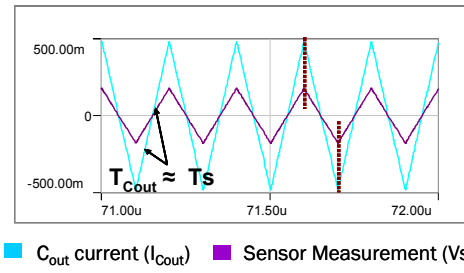


Figure 14. Sensor designed for  $A_{DC}$  of 68 dB but  $A_{DC}$  real of the Op-Amp is 98 dB.

#### IV. EXPERIMENTAL VALIDATION

The design specifications for the experimental validation are: a discrete buck converter switching at 5 MHz,  $C_{out} = 4 \mu F$  ( $4 \cdot 1 \mu F$ ),  $V_{in} = 3 V$ ,  $V_{out} = 1 V$ ,  $R_{load} = 2 \Omega$ . The design of the control loops is presented in [24]. This control has a very fast transient response at constant switching frequency (voltage step from 1.5 V to 2.5 V and 2.5 V to 1.5 V in 2  $\mu s$ ). Also, the response of this control to load step is really fast thanks to the hysteretic control.

Figure 15 validate the design methodology of the current sensor design. It also shows that the sensor measurement ( $V_s$ ) and the  $I_{Cout}$  current are in phase and with scaled impedances.

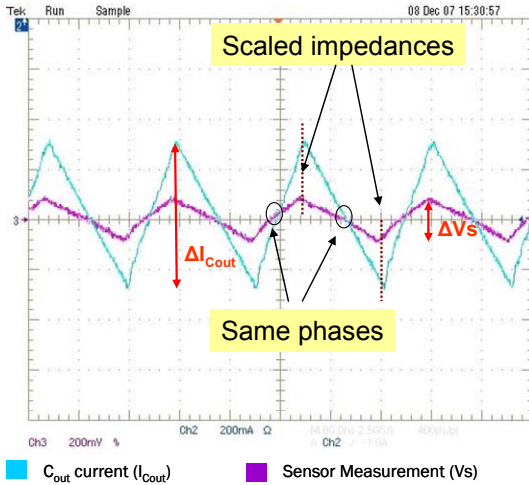


Figure 15. Experimental measurement of sensor. Waveforms for the  $V_s$  and  $I_{Cout}$  have the same time constants and scaled magnitudes.

Figure 16 shows a very fast voltage step from 1.5 V to 2.5 V and 2.5 V to 1.5 V in 2  $\mu s$ .  $V_s$  is the output of the current sensor and it shows an appropriate current measurement for a fast transient response. Therefore, experimental results validate the current sensor design for a very fast transient response.

Figure 17 shows the regulation under 45 A/ $\mu s$  load step. Under a 1 A load steps the output voltage deviation is approximately 50 mV being the output capacitance only 4  $\mu F$

(4  $\cdot 1 \mu F$ ). Therefore, the response of the current sensor is validated under aggressive load steps.

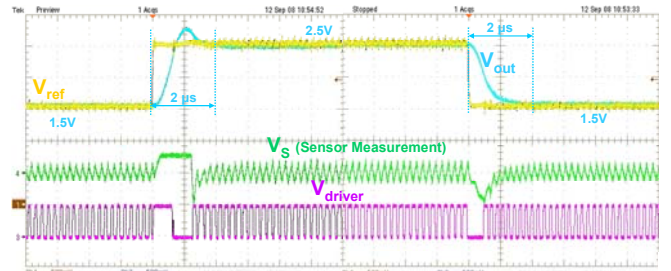


Figure 16. Voltage step ( $V_{ref}$ ) from 1.5V to 2.5V within 2  $\mu s$  (1  $\mu s/div$ ),  $V_{out}$  (500 mV/div),  $V_s$  (2 A/div).

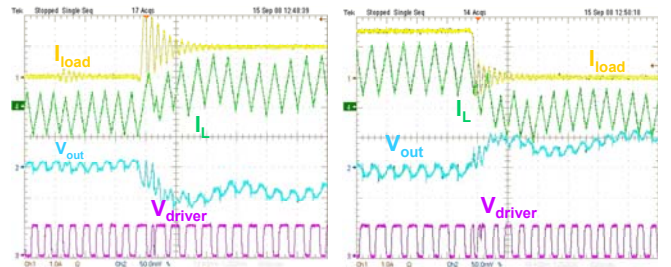


Figure 17. Output voltage regulation under a 45 A/ $\mu s$  load step (400 ns/div),  $V_{out}$  (50 mV/div),  $I_{load}$  (1 A/div),  $I_L$  (1 A/div).

#### V. CONCLUSIONS

This paper presents a design methodology for a non-invasive sensor of the capacitor current. The sensing circuit is designed to mirror the actual capacitor current with a trans-impedance amplifier by matching phase and scaling the impedance of the output capacitor ( $C$ , ESR and ESL).

The sensor includes a trans-impedance amplifier whose input impedance behaves like an inductive and resistive series network that provides the inductive ( $L_i$ ) behavior required to match the ESL. Tolerance, sensor limitations and internal stability of the Op-Amp are considered in the design procedure. Applying the proposed design methodology, values for the parameters  $K_c$ ,  $R_s$  and  $C_s$  are determined and an operational amplifier with adequate characteristics of  $\Delta B$  and  $A_{DC}$  is selected. Simulation and experimental results validate the

proposed design methodology. Tolerances of the system produce mismatch in the time constants of the sensor, however the control technique is robust and operates properly. Experimental results show that this current sensor is appropriate to achieve a very fast dynamic response in Buck derived converters (step voltage from 1.5 V to 2.5 V and 2.5 V to 1.5 V in 2  $\mu$ s). Also, the response of the current sensor under load steps is experimentally validated.

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